Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL/MAY 2026

Sixth Semester

Electronics and Communication Engineering

CEC334 - Analog IC Design

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No.	*Questions*	*BLT*	*CO*	*Marks*
1.	Compare the characteristics of CS, CG and CD.	L2	1	2
2.	What is meant by voltage swing?	L1	1	2
3.	State Miller's theorem.	L2	2	2
4.	Define CMRR.	L1	2	2
5.	List the properties of negative feedback.	L1	3	2
6.	State slew rate.	L2	3	2
7.	Define phase margin.	L1	4	2
8.	What is frequency compensation?	L1	4	2
9.	Outline the faults in logic circuits.	L2	5	2
10.	List the disadvantage of two-clock partial scan.	L1	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a	Enumerate the process source follower using small signal equivalent circuit and derive the voltage gain and output resistance. Also draw the input-output characteristic.	L3	1	16
		Or			
	b	Enumerate the process of cascode stage using small signal equivalent circuit and derive the voltage gain and output resistance.	L3	1	16
12.	a	Explain the high frequency analysis of common source MOSFET amplifier and derive the transfer function.	L2	2	16
		Or			
	b	Briefly explain the statistical characteristics of noise.	L2	2	16
13.	a	Design a circuit that contains two stages of Op Amps and discuss on its parameters.	L3	3	16
		Or			
	b	Design the two-stage op amp circuit for V_{DD} = 1V, P = 1mW, a differential output swing of 1 V_{pp} and a gain of 100. the device parameters assume that $\mu_n C_{ox}$ = 60 $\mu A/V^2$, $\mu_p C_{ox}$ =30 $\mu A/V^2$, λ_n = 0.1V^{-1}, λ_p = 0.2V^{-1} (for an effective channel length of 0.5 µm), γ = 0, V_{THN} = 0.3 V and V_{THP} = −0.35 V.	L3	3	16

14.	a	Explain the compensation of two stage op amps with neat diagram.	L2	4	16
		Or			
	b	Briefly describe the characteristics of slewing in two stage op amps.	L2	4	16
15.	a	Explain the following concepts of fault detection: i. Controllability and Observability ii. Undetectable Faults iii. Equivalent Faults iv. Temporary Faults	L2	5	16
		Or			
	b	Illustrate the following level sensitive scan design: i. Clocked Hazard-Free Latches ii. Double-Latch and Single-Latch LSSD	L2	5	16